CLAIMS

What is claimed is:

1. A method for forming shallow contact interconnects to achieve improved patterning, etching and metal filling characteristics comprising the steps of:

providing a semiconductor substrate comprising CMOS devices including active contact regions;

forming a first set of dielectric layers to form a first thickness for etching a first set of openings through a thickness thereof comprising a bottom portion having a maximum width of less than about 70 nanometers;

etching the first set of openings to contact active contact regions;

filling the first set of openings with a first metal;

forming a second set of dielectric layers to form a second thickness for etching a second set of openings through the second thickness comprising a bottom portion having a maximum width of less than about 70 nanometers;

etching the second set of openings to provide electrical communication with the first set of openings; and,

filling the second set of openings with a second metal to form contact interconnects.

2. The method of claim 1, further comprising the step forming a metallization layer over the contact interconnects in electrical communication with at least a portion of the contact interconnects.

3. The method of claim 1, wherein the first and second set of openings have an aspect ratio with respect to the bottom portion of less than about 3.3.

4. The method of claim 1, wherein the first and second set of openings have an aspect ratio with respect to the bottom portion of less than about 4.5.

5. The method of claim 4, wherein the bottom portion has a width of less than about 50 nm.

6. The method of claim 1, wherein the first and second set of dielectric layers comprises PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, silicon oxynitride, or combination thereof.

7. The method of claim 1, wherein the first and second set of dielectric layers comprise lowermost portions selected from the group consisting of silicon carbide, nitrogen doped silicon oxide, silicon nitride, and silicon oxynitride.

8. The method of claim 7, wherein the first and second set of dielectric layers comprise overlying portions selected from the group consisting of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, and fluorine doped silicon oxide.

9. The method of claim 1, wherein the first and second metals are selected from the group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta.

10. The method of claim 1, wherein the active contact regions are selected from the group consisting of source and drain regions and gate electrodes.

11. The method of claim 10, wherein the active contact regions comprise a conductive material selected from the group consisting of Ti, Co, Ni, Pt, W, $TiSi_2$, $CoSi_2$, NiSi, PtSi, WSi_2, TiN, and TaN.

12. The method of claim 1, wherein the first and second set of dielectric layers comprises an uppermost portion selected from the group consisting of a hardmask layer and a BARC layer.

13. The method of claim 1, wherein the steps of etching a first and second set of openings comprise forming and patterning one or more resist layers selected from the group consisting of organic resists and inorganic containing resists.

14. The method of claim 13, wherein the one or more resist layers have a thickness of between about 0.15 microns and about 1.0 microns.

15. The method of claim 1, wherein the first and second sets of openings comprise a shape selected from the group consisting of circular and rectangular.

16. The method of claim 1, wherein the first and second set of openings are selected from the group consisting of butt contact openings, openings having a length horizontal to the semiconductor substrate major surface between about 0.15 microns to about 500 microns.

17. The method of claim 1, wherein the contact interconnects are selected from the group consisting of vias, contact holes, butt contact interconnects, local interconnects, and interconnect lines.

18. A contact interconnect structure comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first set of dielectric layers comprising a first contact layer overlying the active contact regions comprising a first plurality of metal filled openings extending through the first contact layer thickness to provide electrical communication to the active contact regions;

a second set of dielectric layers comprising a second contact layer overlying the first contact layer comprising a second plurality of metal filled openings extending through the first contact layer thickness to provide electrical communication to the first contact region;

wherein, each of the first and second plurality of metal filled openings comprise a bottom portion having a maximum width of less than about 70 nanometers and an aspect ratio of less than about 4.5.

19. The contact interconnect structure of claim 18, wherein the bottom portion has a maximum width of less than about 50 nanometers and an aspect ratio of less than about 4.5.

20. The contact interconnect structure of claim 18, further comprising an overlying metallization layer in electrical communication with the second contact layer.

21. The contact interconnect structure of claim 18, wherein the first and second set of dielectric layers comprises PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, silicon oxynitride, or combination thereof.

22. The contact interconnect structure of claim 18, wherein the first and second set of dielectric layers comprise lowermost portions selected from the group consisting of silicon carbide, nitrogen doped silicon oxide, silicon nitride, and silicon oxynitride.

23. The contact interconnect structure of claim 18, wherein the first and second set of dielectric layers comprise overlying portions selected from the group consisting of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, and fluorine doped silicon oxide.

24. The contact interconnect structure of claim 18, wherein the first and second first and second plurality of metal filled openings comprise conductive materials selected from the group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta.

25. The contact interconnect structure of claim 18, wherein the active contact regions are selected from the group consisting of source and drain regions and gate electrodes.

26. The contact interconnect structure of claim 18, wherein the gate electrode comprises a gate structure having a gate length of less than about 45 nm.

27. The contact interconnect structure of claim 18, wherein the active contact regions comprise a conductive material selected from the group consisting of Ti, Co, Ni, Pt, W, $TiSi_2$, $CoSi_2$, NiSi, PtSi, WSi_2, TiN, and TaN.

28. The contact interconnect structure of claim 18, wherein the first and second set of dielectric layers comprises an uppermost portion selected from the group consisting of a hardmask layer and a BARC layer.

29. The contact interconnect structure of claim 18, wherein the first and second plurality of metal filled openings comprise a shape selected from the group consisting of circular and rectangular.

30. The contact interconnect structure of claim 18, wherein the first and second first and second first and second plurality of metal filled openings are selected from the group consisting of vias, contact holes, butt contact interconnects, local interconnects, and interconnect lines.

31. The contact interconnect structure of claim 30, wherein the interconnect lines have a length horizontal to the semiconductor substrate major surface between about 0.15 microns to about 500 microns.

32. A contact interconnect structure comprising:

at least a first contact layer comprising a first plurality of metal filled openings extending through the first contact layer thickness to provide electrical communication to overlying and underlying conductive regions;

wherein, the first plurality of metal filled openings comprise a bottom portion having a maximum width of less than about 70 nanometers and an aspect ratio of less than about 3.3.

33. The contact interconnect structure of claim 32, wherein the bottom portion has a maximum width of less than about 50 nanometers and an aspect ratio of less than about 4.5.

34. The contact interconnect structure of claim 32, wherein the at least a first contact layer comprises one of an overlying an underlying second contact layer.

35. The contact interconnect structure of claim 32, wherein the underlying conductive regions comprise active conductive regions selected from the group consisting of source and drain regions and gate electrodes.

36. The contact interconnect structure of claim 35, wherein the gate electrode comprises a gate structure having a gate length of less than about 45 nm.

37. The contact interconnect structure of claim 32, wherein the overlying conductive regions comprise a metallization layer.